

WHAT IS CLAIMED IS:

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1. A method of transferring data through a bus, comprising the steps of:

occupying the bus by a first device serving as a bus master;

transferring a first predetermined number of data items of all data items to be transferred while the first device is occupying the bus;

determining if the first predetermined number of data items have been transferred;

determining if the first device should release the bus based on whether or not there is a request from a second device after it is determined that the first predetermined number of data items have been transferred; and

releasing the bus by the first device when it is determined that the first device should release the bus.

2. A method of transferring data through a bus according to claim 1, further comprising the steps of:

occupying the bus by the second device serving as the bus master after the first device releases the bus;

releasing the bus by the second device after the second device completes access to the bus;

occupying the bus again by the first device after the second device releases the bus; and

transferring a second predetermined number of data items subsequent to the first predetermined number of the data items which have been transferred while the first device is occupying the bus again.

3. A method of transferring data through a bus according

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to claim 1, further comprising the step of, when it is determined that the first device should not release the bus, transferring by the first device a second predetermined number of data items subsequent to the first predetermined number of the data items which have been transferred while the first device continues to occupy the bus.

4. A method of transferring data through a bus according to claim 1, further comprising the steps of:

determining if all the data items to be transferred have been transferred; and

releasing the bus after it is determined that all the data items to be transferred have been transferred.

5. A method of transferring data through a bus according to claim 1, wherein:

the first device is a DMA controller; and
the second device is a CPU.

6. A bus master control device for controlling an operation of a bus master for transferring data through a bus, the device comprising:

bus occupation request means for outputting a signal requesting to occupy the bus in response to a data transfer request;

data transfer means for transferring a first predetermined number of data items of all data items to be transferred while the bus master is occupying the bus; and

bus release instruction means for outputting a signal instructing to release the bus after the first predetermined number of data items have been transferred.

7. A bus master control device according to claim 6, wherein:

the bus occupation request means outputs again the signal requesting to occupy the bus after the bus release instruction means outputs the signal instructing to release the bus; and

the data transfer means transfers a second predetermined number of data items subsequent to the first predetermined number of the data items which have been transferred while the bus master is occupying the bus again.

8. A bus master control device according to claim 6, wherein the bus release instruction means outputs the signal instructing to release the bus after all the data items to be transferred have been transferred.

9. A bus master control device according to claim 6, the data transfer means comprising:

a first counter for counting a number of data items which have been transferred out of the first predetermined number of data items; and

first determination means for determining if the first predetermined number of data items have been transferred based on an output from the first counter.

10. A bus master control device according to claim 9, the data transfer means comprising:

a second counter for counting a number of data items which have been transferred out of all the data items to be transferred; and

second determination means for determining if all the data items to be transferred have been transferred

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based on an output from the second counter.

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